The Fedora Project is out front for you, leading the advancement of free, open software and content.

fedora

Electronic Lab

Chitlesh GOORAH

Design tools for

- Analog/Digital Simulation
- Circuit Simulation
- Verification and Documentations
- Hardware Development
- Micro Controller (µC) Programming
- Embedded Systems Development

A simulation platform for Micro-Nano Electronics Engineering and Embedded Systems

Requirements:

fedora

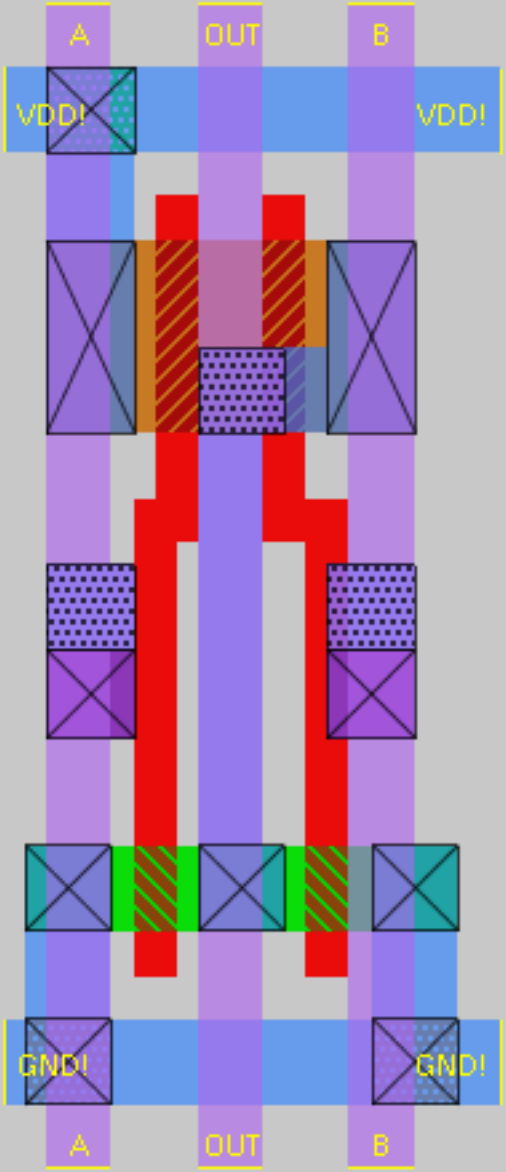
Fedora is a Linux-based OS.

Introduces:

- tools for Application-Specific Integrated Circuit (ASIC) Design Flow process.
- extra open source standard cell libraries supporting a feature size of 0.13µm.
- extracted spice decks which can be simulated with any spice simulators.
- interoperability between packages, to achieve different design flows.

File Options DRC=0 Loaded: nor Editing: nor Tool: box (-35 59) -92 38 lambda

VLSI Design Layout & Checks



Continuous DRC that operates in background

Hierarchical circuit extractor

Routing tools that work under and around existing connections.

Dedicated to training in sub-micron CMOS VLSI design

Supports technology files by the MOSIS foundry service.

Switch-level simulation of the layout,

- Transistors as ideal switches
- RC time constants

Generates GDS II stream format and Caltech Intermediate Form (CIF)

(Achievement : Thick-film circuit layout using the Magic layout editor.)

Digital Design

Hardware Description Languages

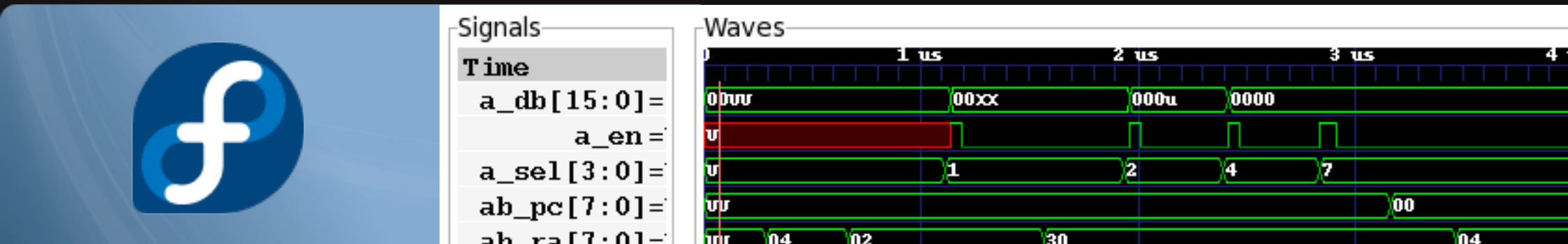
A HDL simulation environment that enables you to verify the functional and timing models of your design.

Achievements:

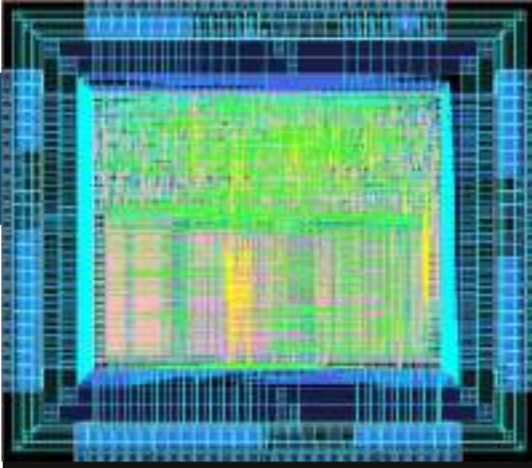
Successfully compiled and run
— a DLX processor and
— a LEON1 SPARC processor.

Key Features:

Supports both VHDL and Verilog designs.
A graphical waveform viewer.
A Verilog simulator and synthesis tool for IEEE 1364-2001 standard.

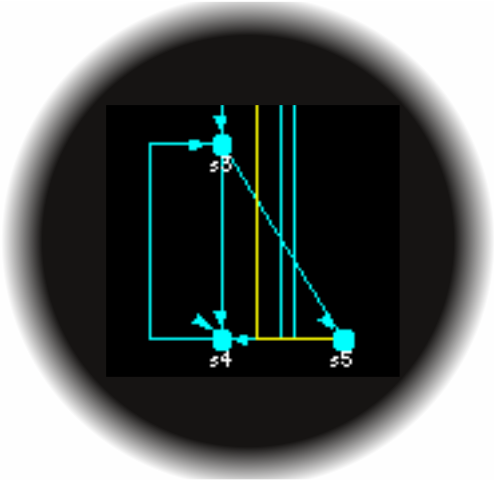


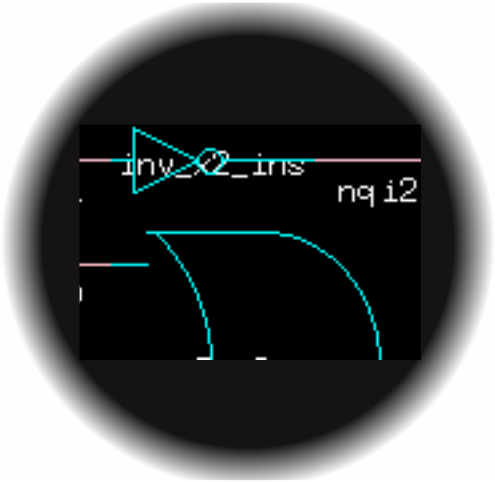
RTL and logic synthesis design flows.



Automatic schematic generation

VHDL compilation and simulation

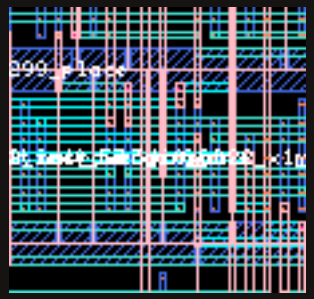




Physical optimization and layout design flows.

7 extra standard cells up to a feature size of 0.13µm

Read/write standard ins/outs including Verilog® and VHDL.

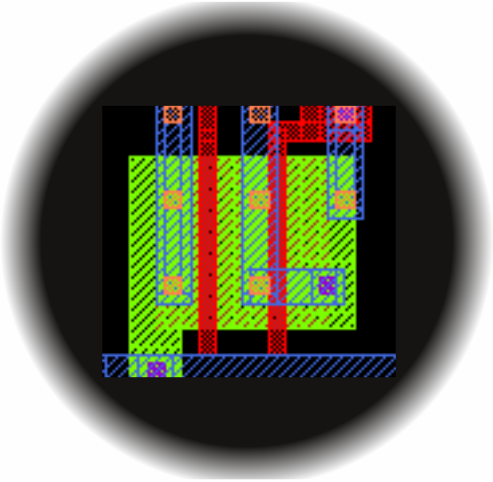


Place and route,

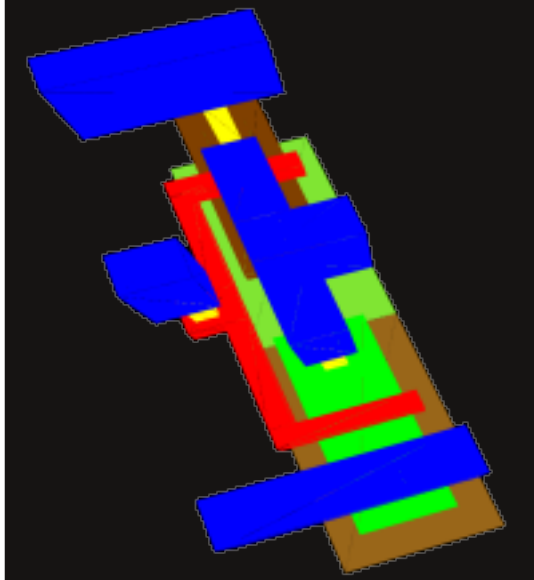
Layout edition,

Automatic Layout generation

Netlist extraction and verification



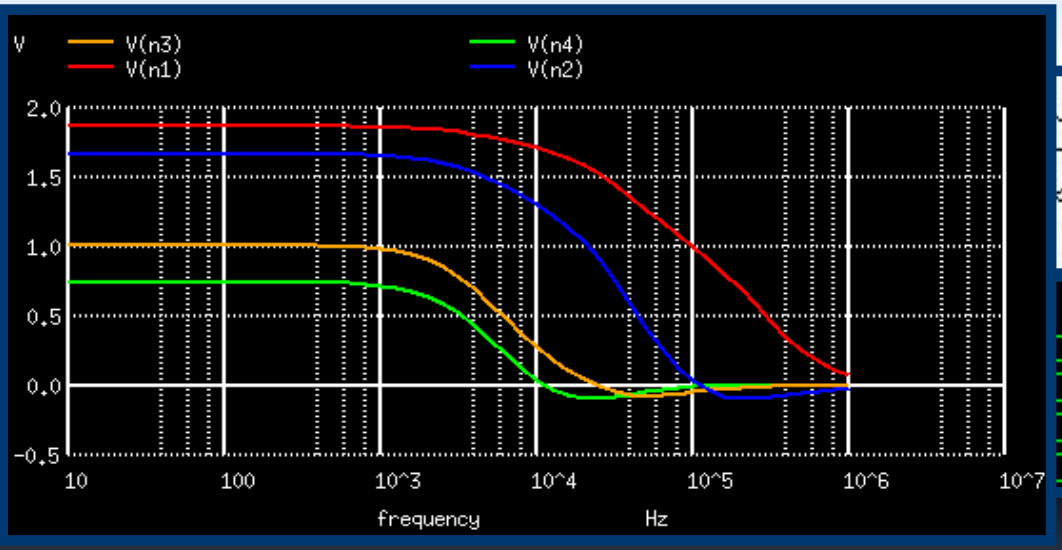
Creates a POV-Ray (3D view) scene description file of the GDSII data.

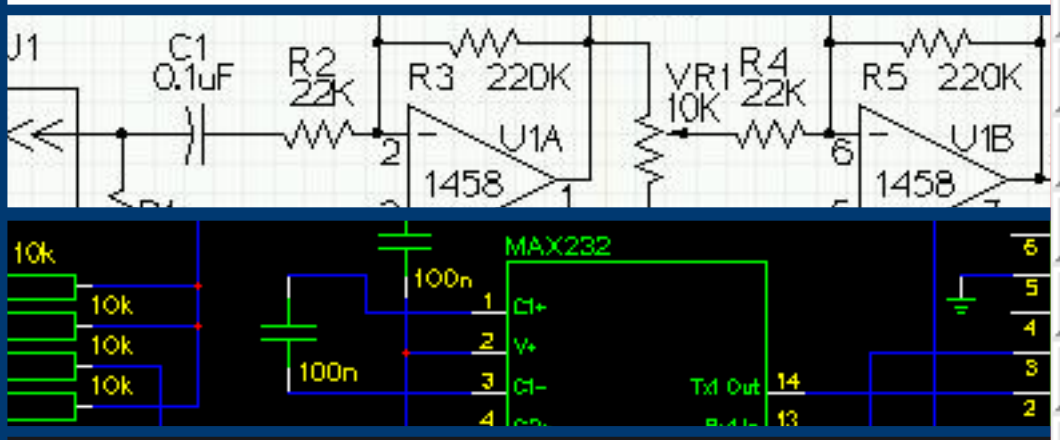


Circuit Simulation

– General Purpose Circuit Simulators
  - o Nonlinear AC/DC analysis
  - o Transient, Fourier analysis

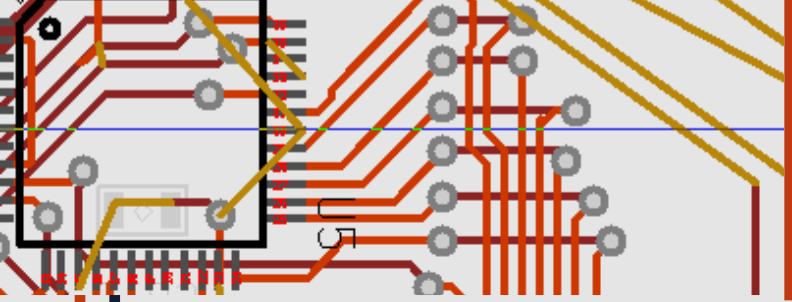
– Beyond Spice capabilities: Level 49, BSIMv3 and EKV implementations





– Draws publishable-quality electrical circuit schematic diagrams.
– Circuit components can be retrieved from libraries which are fully editable.
– Easy-to-use GUI with TCL interface or GTK interface.

PCB Layout Design



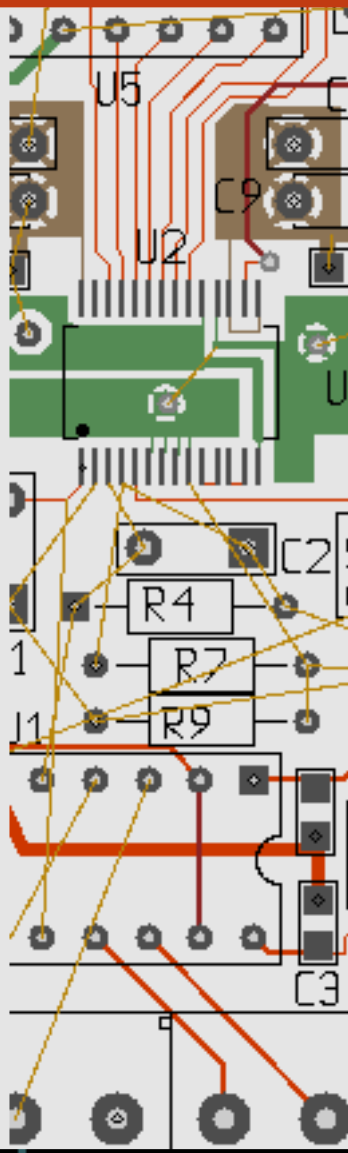
A professional-quality printed circuit board design environment along with :

- o schematic capture, simulation,
- o netlisting into over 20 netlist formats.

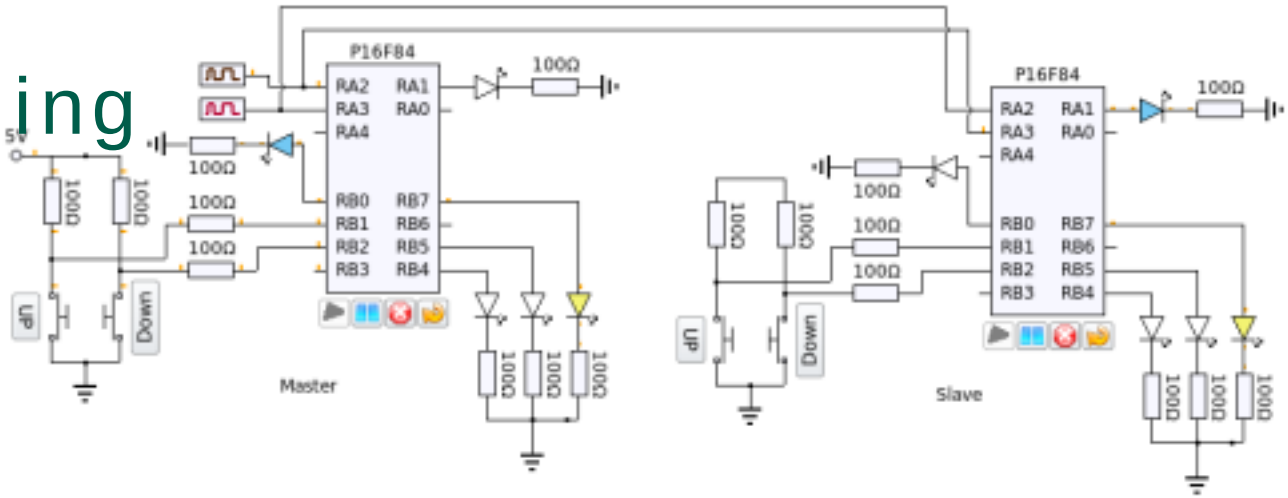
Design rule checking
Industry standard RS-274-X (Gerber), NC drill, etc.

Offers high end features such as an autorouter and trace optimizer, which can tremendously reduce layout time.

PCB of up to 16 layers with an unlimited number of components and nets.
Viewer for Gerber files (RS274X),



µController Programming



Small Device C Compiler, the GNU PIC Utilities, the PICC compilers, etc.
Ease to use IDEs for microcontrollers circuit design, simulation and programmation to serial, parallel and USB ports.

Supported debuggers
Supports 8051 and AVR.

AVR Development System

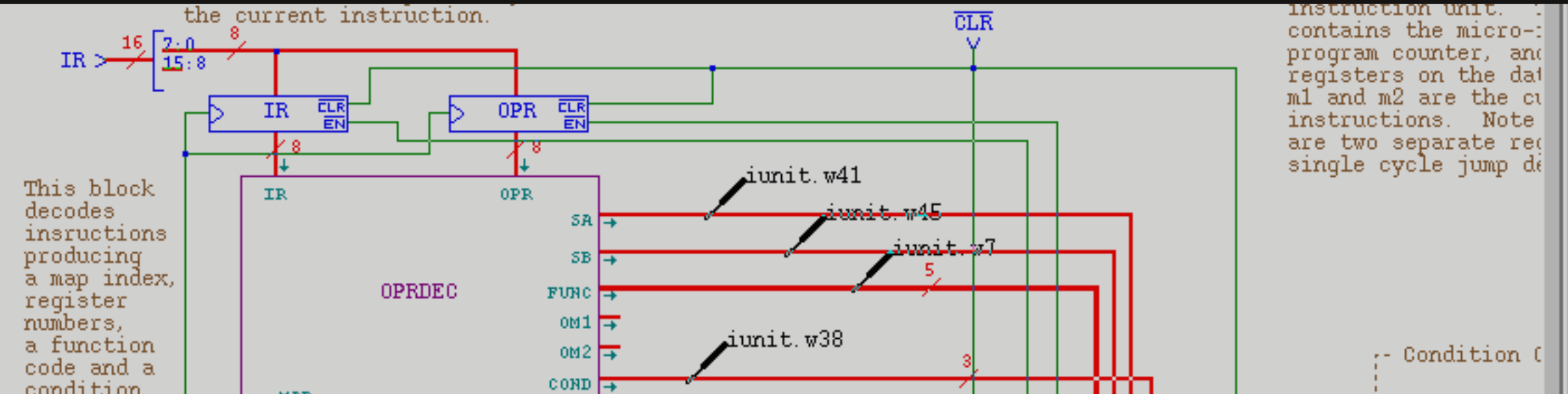
Supports the Atmel's STK500-like programmers
- Cross compilers
- a Program for interfacing the Atmel JTAG ICE to GDB
- Small Device C Compiler

Embedded Systems Development

What is coming in a near future ?

- Tkgate

  Graphical circuit design
  Logic simulation
   Graphical display of simulation results.
   Breakpoints, single-step and clock-step simulator control
  Basic gates
  ALU components



What is coming in a near future ?

- Tclspice

"We try to act in concert with the following independent Open-Source EDA efforts to achieve (eventually) a complete freely available but industrial quality tool-set which work together seamlessly."

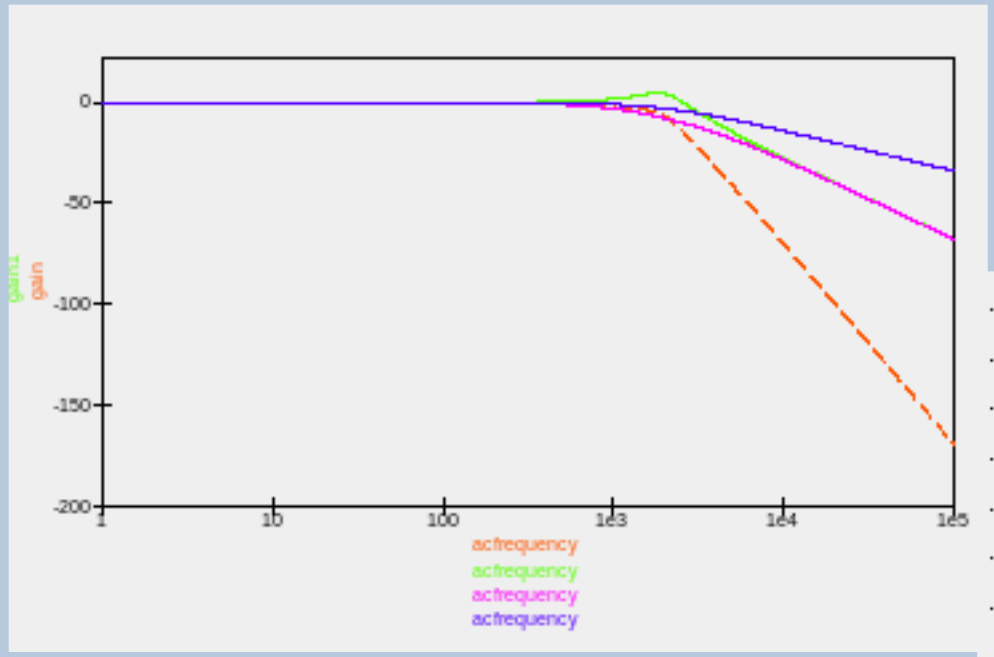
Are concerned :

- Magic VLSI editor
- Xcircuit schematic capture package
- Automatic Schematic Generation
- FastHenry Inductance extractor
- FastCap Capacitance field solver
- OpenAccess VLSI database
- Octtools, TimberWolf, place / router

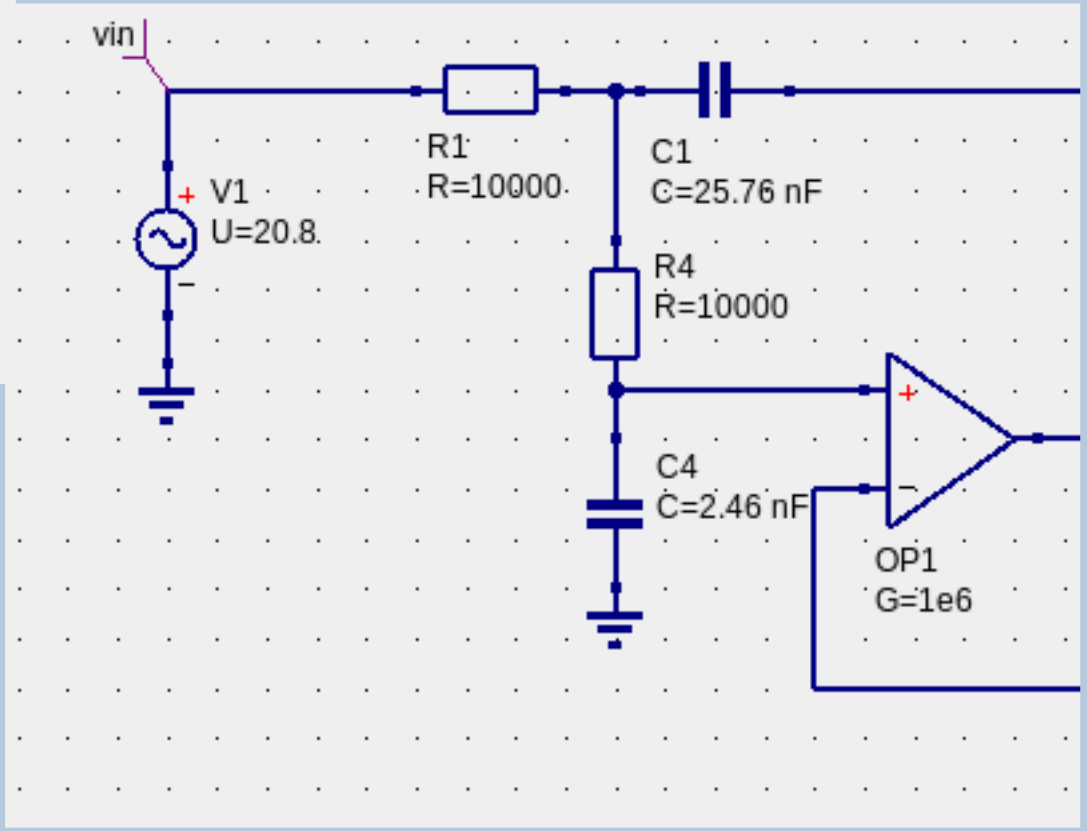
A company behind :

MultiGiG ltd

Circuit Simulation with Qucs

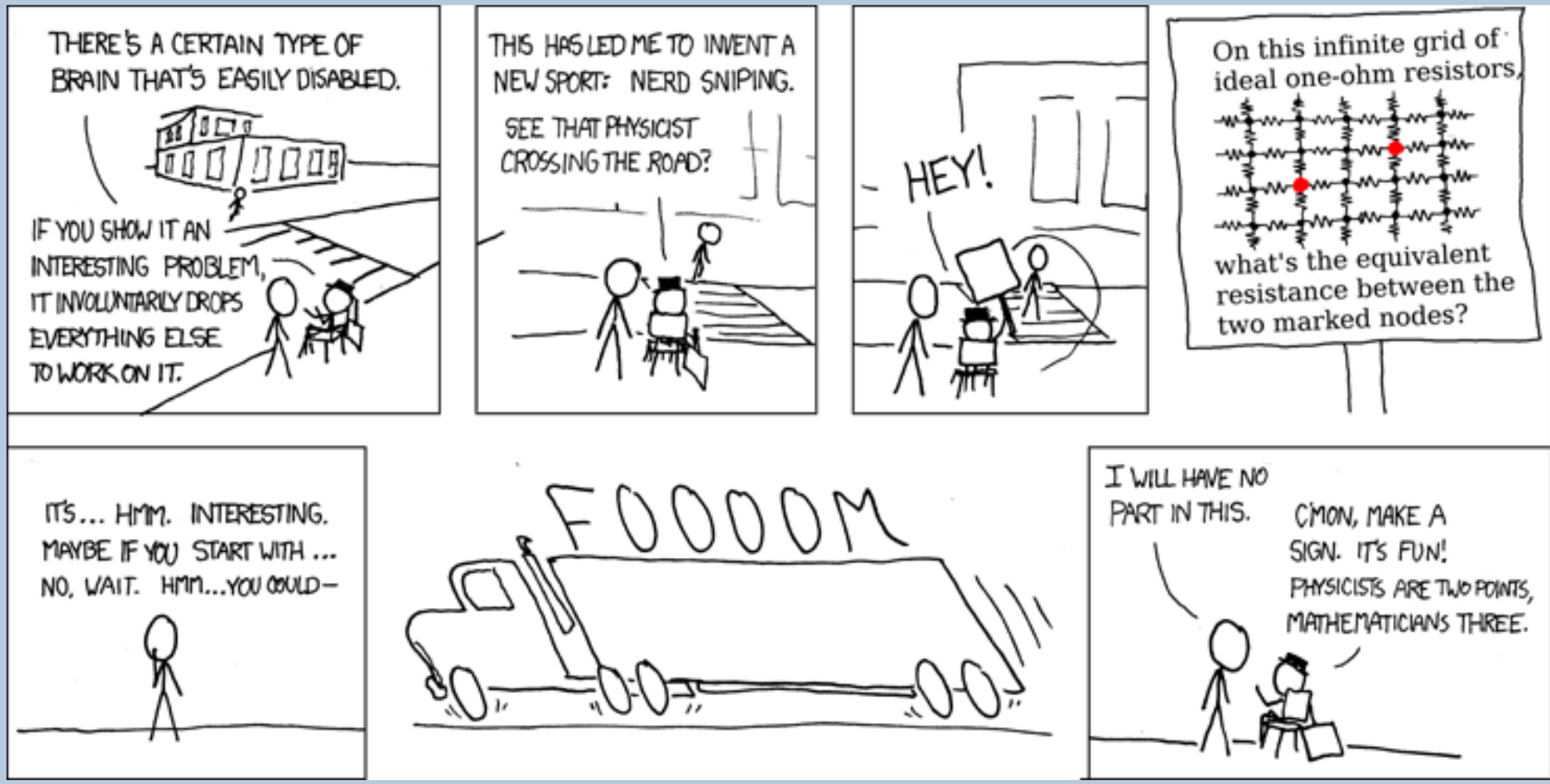


Butterworth filter, order 5



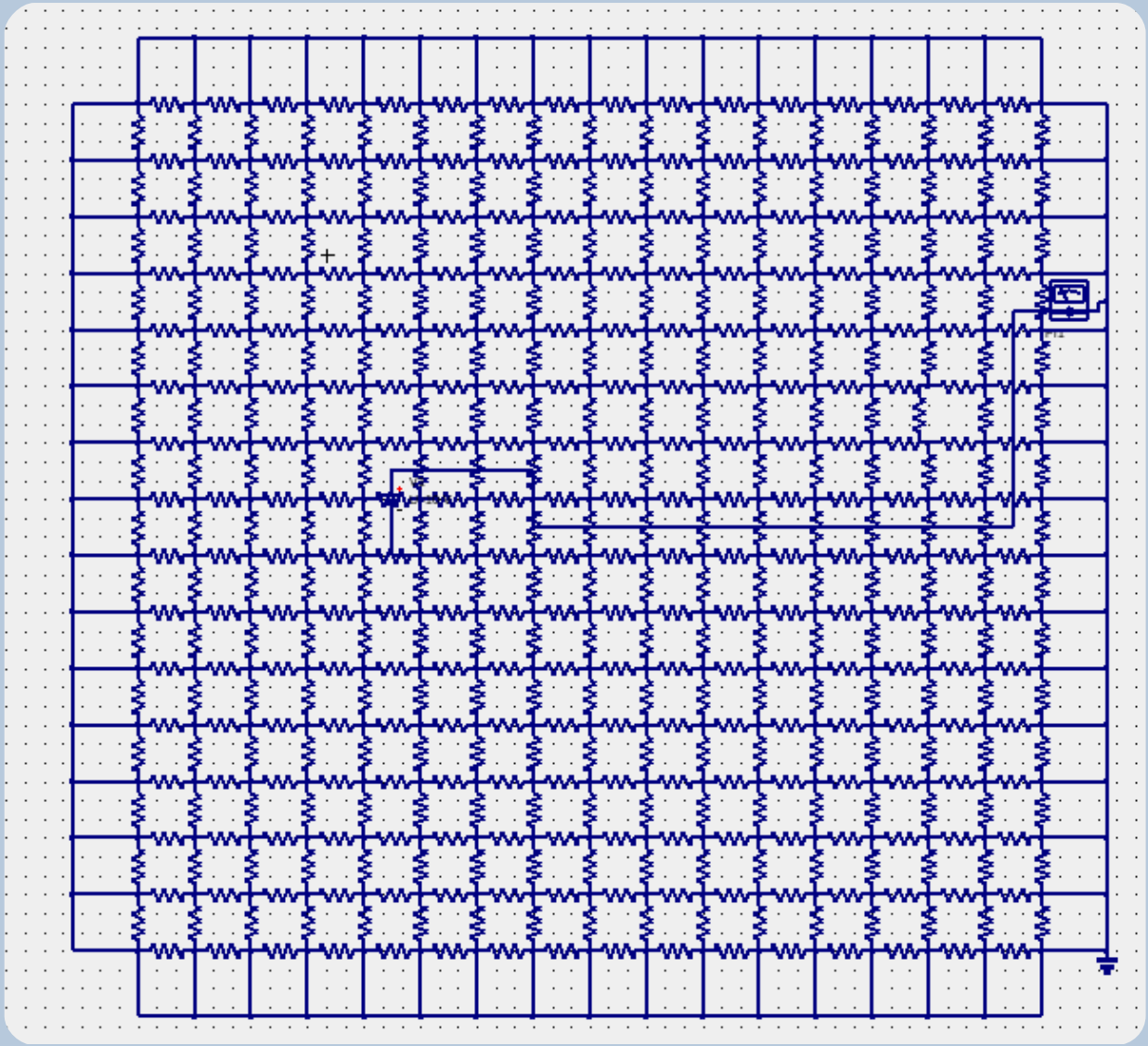
Circuit Simulation with Qucs

Know this xkcd ?



Source : http://www.xkcd.org

Circuit Simulation with Qucs



- Equivalent resistance : 0.77 Ohm

- Copy and paste make it easy to design

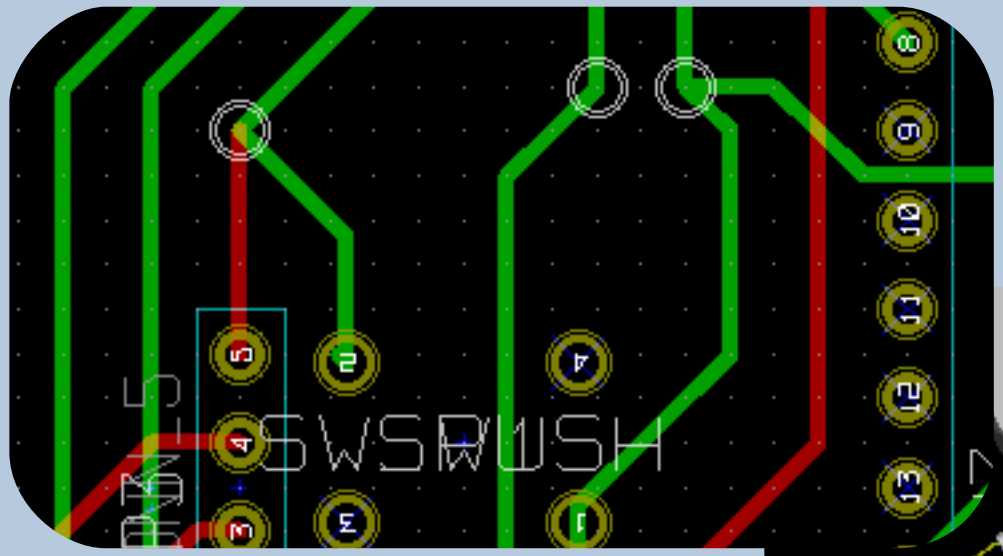
- Intuitive interface

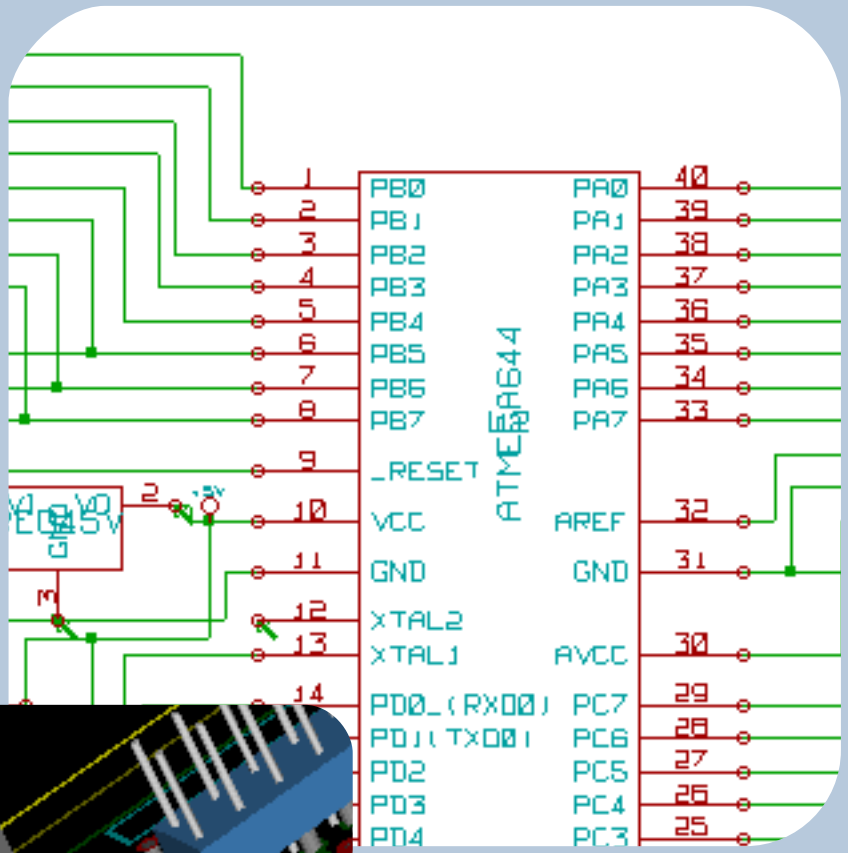
- 2D and 3D Plots

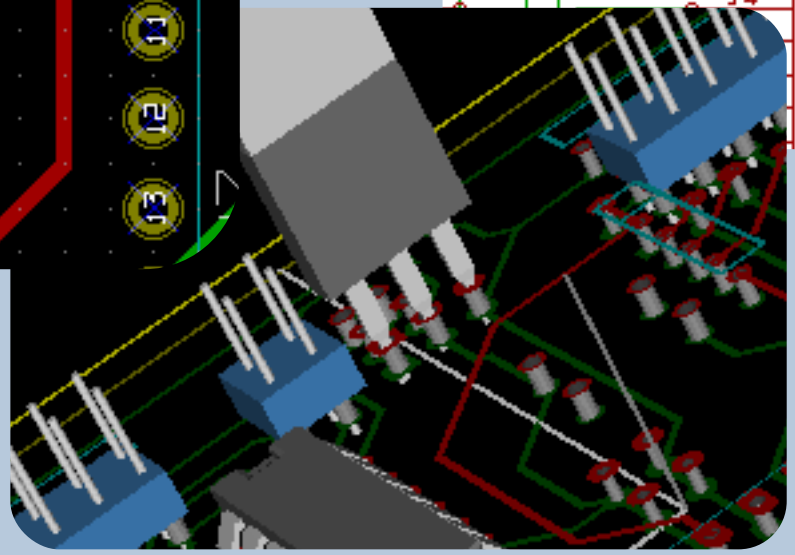
PCB design & Microcontroler programming

Example project : ASAP
(ASAP is Simply an Avr Project)

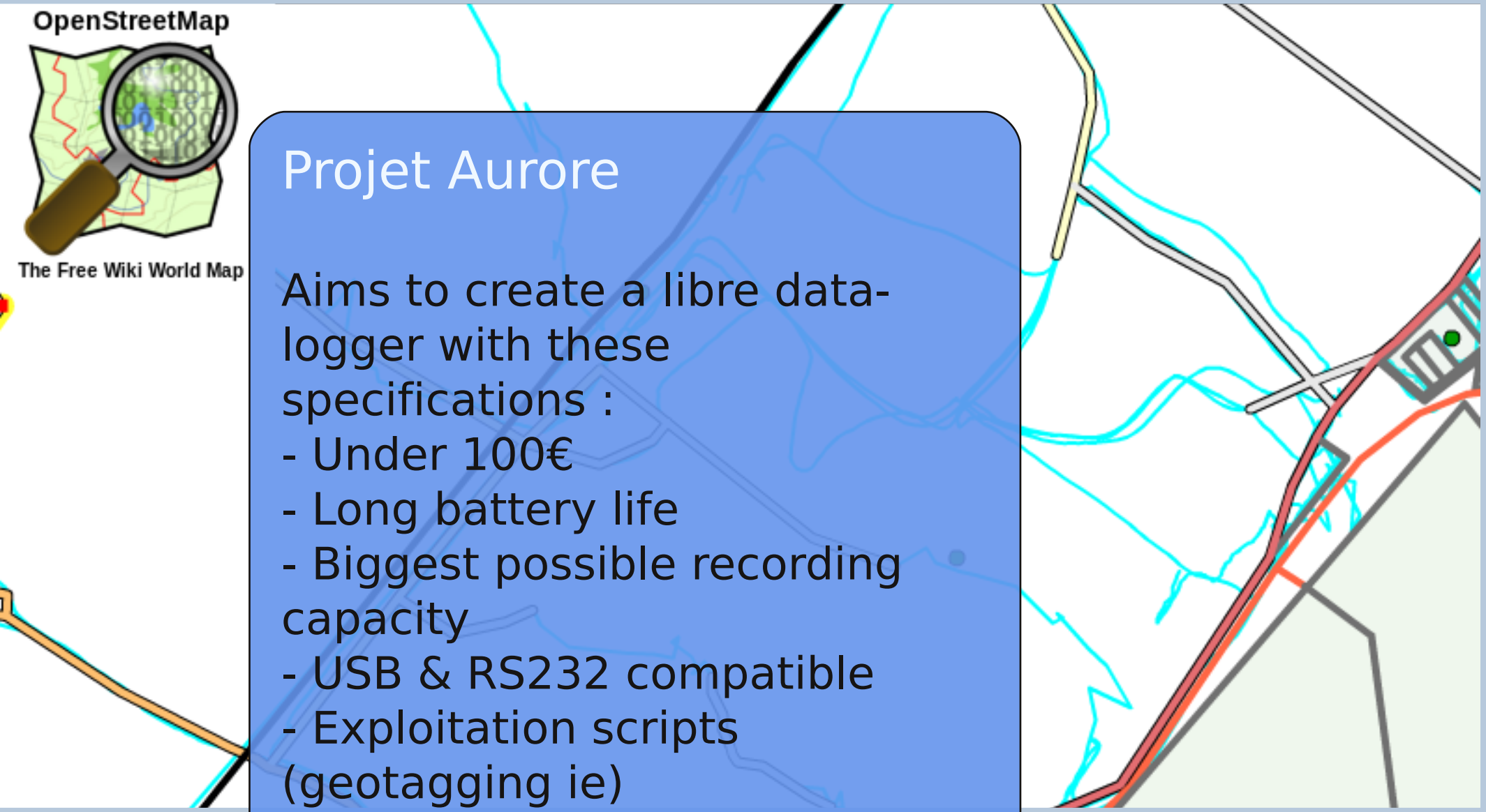
Uses Kicad







PCB design & Microcontroler programming

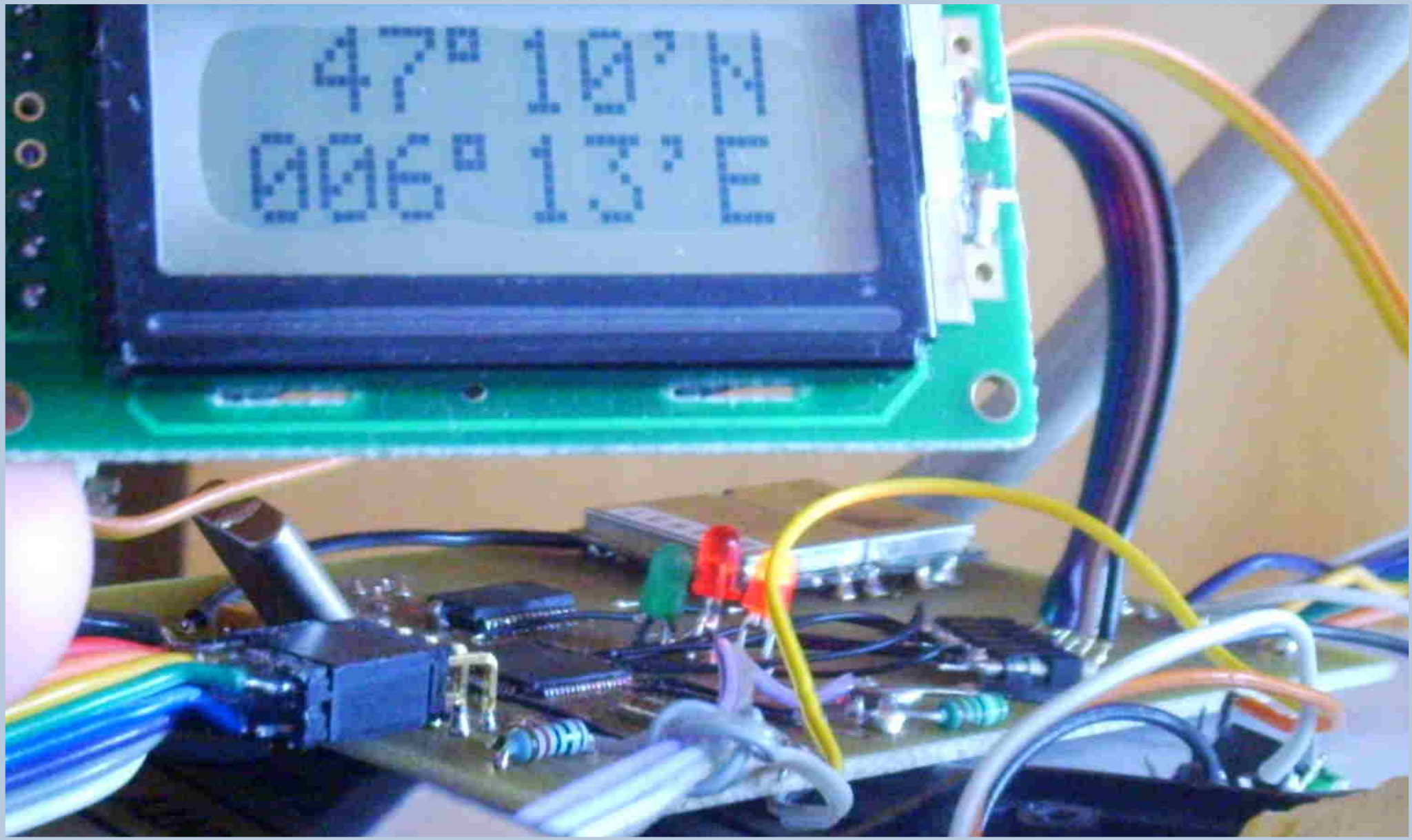


Projet Aurore

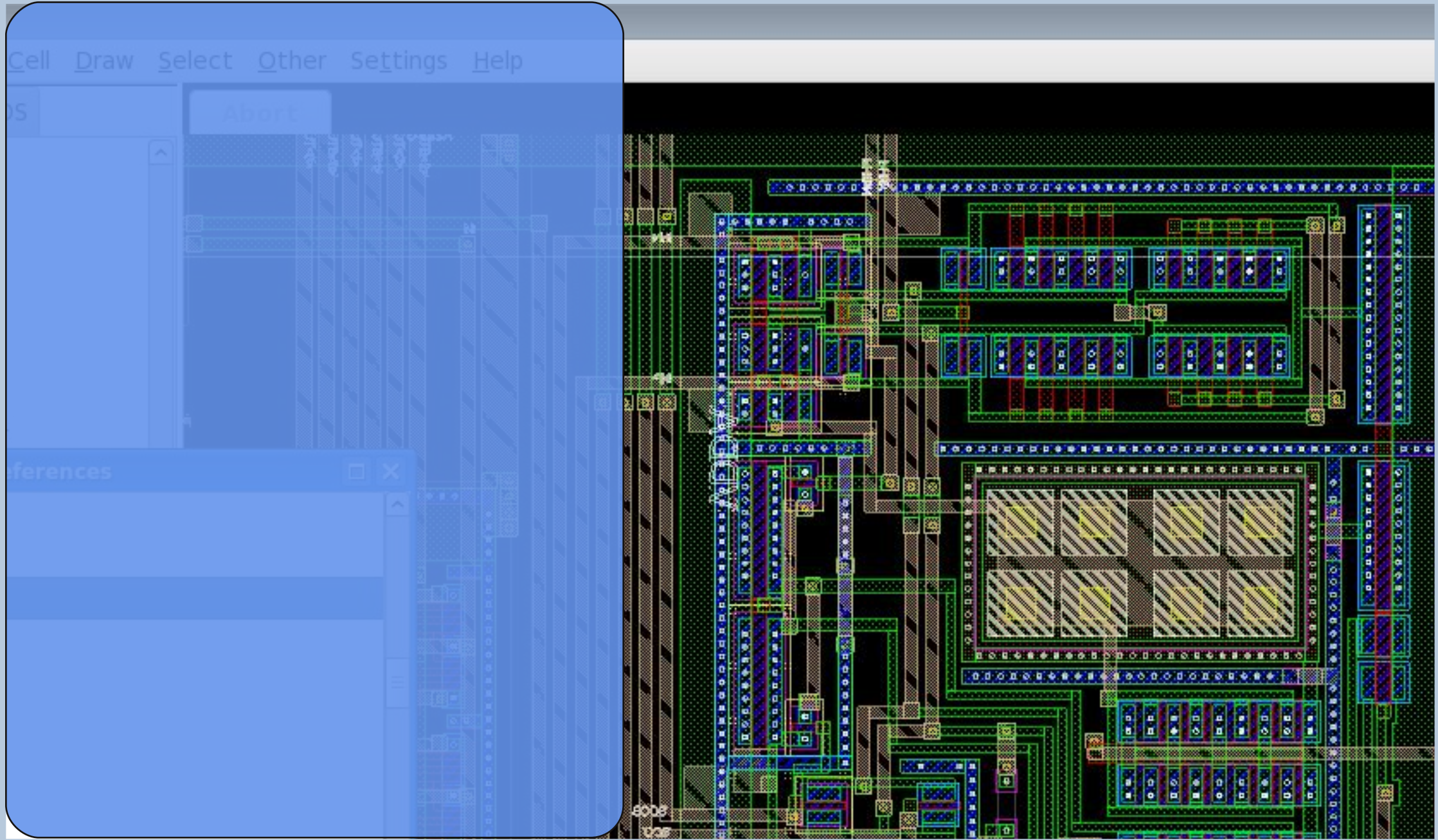
Aims to create a libre data-logger with these specifications :

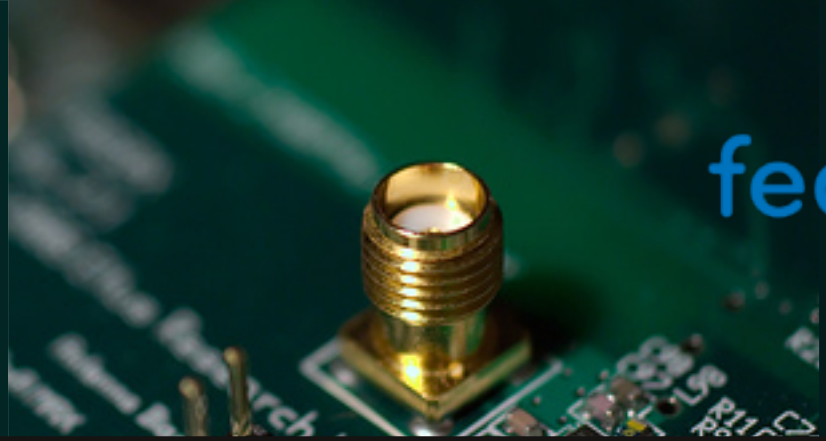
- Under 100€
- Long battery life
- Biggest possible recording capacity
- USB & RS232 compatible
- Exploitation scripts (geotagging ie)

PCB design & Microcontroler programming



IC Layout Editing





fedora Electronic Lab

Fedora is a Linux-based operating system. Fedora is always free for anyone to use, modify, and distribute.

Fedora Electronic Laboratory (FEL) provides a complete electronic laboratory setup with reliable open source design tools as well as project

It can be downloaded freely as a LiveCD via torrent.

Download the latest version 9.

All Fedora Electronic Lab packages can be freely

website :

http://chitlesh.fedorapeople.org/FEL

technical support :

Fedora Users Mailing List

contact:

Chitlesh GOORAH
(Fedora Electronic Lab Architect)

Fedora Embedded SIG

Fedora SciTech SIG